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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,761	06/24/2005	Takashi Watanabe	63645(70820)	9544

21874 7590 04/17/2008
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EXAMINER	
JERABEK, KELLY L	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
04/17/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,761	WATANABE, TAKASHI	
	Examiner	Art Unit	
	KELLY L. JERABEK	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☒ Claim(s) *5-8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This is a first office action in response to application 10/540,761 filed on 6/24/2005 in which claims 1-8 are presented for examination.

Information Disclosure Statement

The information disclosure statements filed on 6/24/2005 and 11/28/2007 are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 are rejected under 35 U.S.C. 102(b) as being anticipated by Masazumi JP 2001-339639.

Re claim 1, Masazumi discloses a solid-state imaging device in which a photodiode (D_{11}, D_{21}, D_{12}, D_{22}) and a first transistor (M_{111}, M_{211}, M_{121}, M_{221}) are provided in series between a ground and a drain in each pixel, and a signal corresponding to a current or an electric charge generated in the photodiode (D_{11}, D_{21}, D_{12}, D_{22}) according to an optical input is outputted from a detection node located between the photodiode (D_{11}, D_{21}, D_{12}, D_{22}) and the first transistor (M_{111}, M_{211}, M_{121}, M_{221}) (page 4, paragraph 19-page 6, paragraph 30; figures 1-2), comprising: a control part (M_{010}, M_{020}) that executes control to alternately repeat a logarithmic operation period during which a photoelectric conversion signal is logarithmically converted by setting a gate voltage of the first transistor (M_{111}, M_{211}, M_{121}, M_{221}) to a first level is obtained and a linear operation period during which a linear photoelectric conversion signal is obtained by setting the gate

voltage of the first transistor (M_{111}, M_{211}, M_{121}, M_{221}) to a second level (page 5, paragraph 23-page 7, paragraph 36).

Re claim 2, Masazumi discloses that the photodiode (D_{11}, D_{21}, D_{12}, D_{22}) and a detection node are connected together (figure 2).

Re claim 3, Masazumi discloses a second transistor (M_{112}, M_{212}, M_{122}, M_{222}) that is connected between the photodiode (D_{11}, D_{21}, D_{12}, D_{22}) and a detection node (figure 2).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Masazumi JP 2001-339639.

Re claim 4, Masazumi discloses all of the limitations of claim 3 above. However, Masazumi fails to specifically state that the photodiodes (D_{11}, D_{21}, D_{12}, D_{22}) have buried-

channel structures. There Examiner takes **Official Notice** that it is well known in the image sensor art for photodiodes to have buried-channel structures. Therefore, it would have been obvious for one skilled in the art to have been motivated to include photodiodes having buried-channel structures in the solid-state imaging device disclosed by Masazumi in order to ensure that the solid-state imaging device is compact in size and is capable of capturing electronic images of acceptable image quality.

Allowable Subject Matter

Claims 5-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Re claims 5-8, the prior art fails to teach or suggest, "A solid-state imaging device in which a photodiode and a first transistor are provided in series between a ground and a drain in each pixel, and a signal corresponding to a current or an electric charge generated in the photodiode according to an optical input is outputted from a detection node located between the photodiode and the first transistor, comprising: a control part that executes control to alternately repeat a logarithmic operation period during which a

photoelectric conversion signal is logarithmically converted by setting a gate voltage of the first transistor to a first level is obtained and a linear operation period during which a linear photoelectric conversion signal is obtained by setting the gate voltage of the first transistor to a second level, wherein the control part executes control so as to alternately repeat the logarithmic operation period and the linear operation period every frame, **read a potential of the detection node as a linear type signal immediately before a transition from the linear operation period to the logarithmic operation period, and read the potential of the detection node as a logarithmic signal in the logarithmic operation period after a lapse of a certain period after the transition to the logarithmic operation period"**.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hagihara et al. (US 2001/0052940) discloses a solid-state image sensing device. The information regarding a logarithmic conversion mode and a linear conversion mode is relevant material.

Watanabe (US 7,102,677) discloses a reduced thermal release effect amplification-type solid imaging device. The information regarding amplification of an image signal in a solid-state imaging device is relevant material.

Contacts

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kelly L. Jerabek whose telephone number is **(571) 272-7312**. The examiner can normally be reached on Monday - Friday (8:00 AM - 5:00 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached at **(571) 272-7372**. The fax phone number for submitting all Official communications is **(571) 273-7300**. The fax phone number for submitting informal communications such as drafts, proposed amendments, etc., may be faxed directly to the Examiner at **(571) 273-7312**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Kelly L. Jerabek/

Examiner, Art Unit 2622

/James M Hannett/

Primary Examiner, Art Unit 2622